Dynamic Partial Reconfiguration for Dependable Systems

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DPR for Dependable systems

- Dynamic Partial Reconfiguration (DPR) is the ability of a programmable device (i.e., FPGA) to dynamically change some of its selected portions while the rest is unchanged and operating

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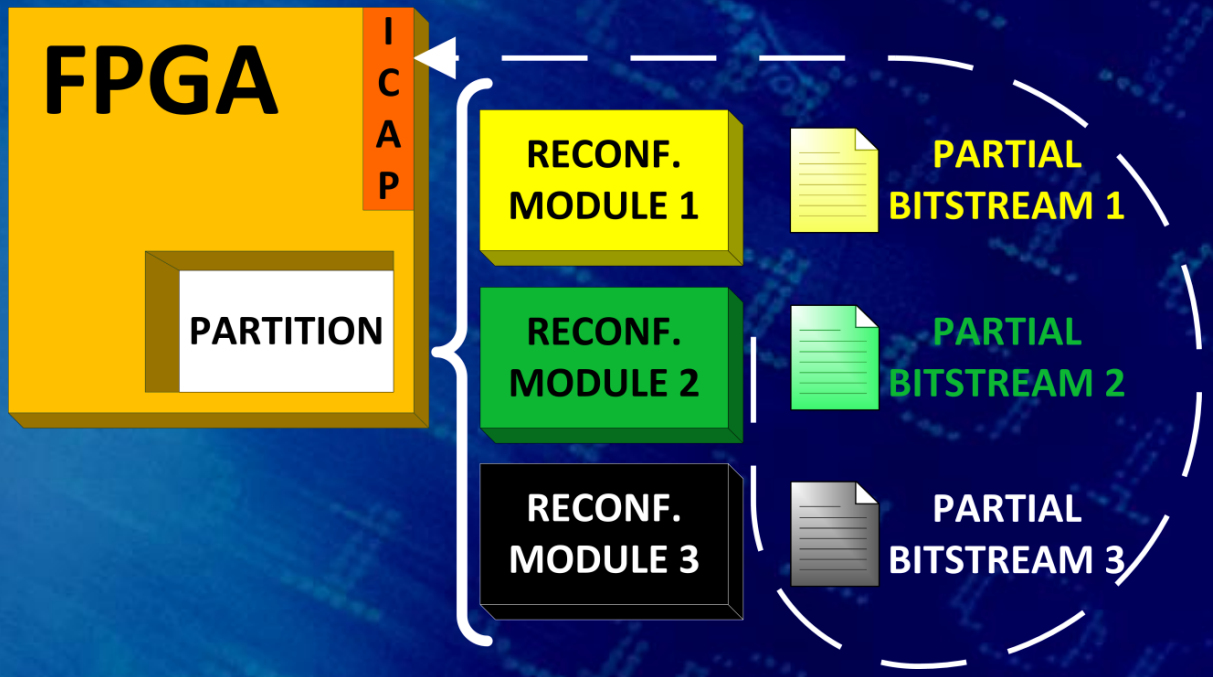


DPR for Dependable systems

- Dynamic Partial Reconfiguration (DPR) is the ability of a programmable device (i.e., FPGA) to dynamically change some of its selected portions while the rest is unchanged and operating
  - Often used to hardware accelerate tasks by on-demand reconfiguration with specific IP-Cores

DPR for Dependable systems

- **Dynamic Partial Reconfiguration (DPR) is the ability of a programmable device (i.e., FPGA) to dynamically change some of its selected portions while the rest is unchanged and operating**

But:

- **Is the DPR process itself dependable?**
- **Is it possible to exploit DPR to improve FPGA robustness by mitigating *Non-functional properties* (i.e., temperature, power, aging) effects?**

Mitigating SEE in DPR process

ISSUE:

- **When performing partial reconfiguration, wrong data can be written in the FPGA configuration memory**

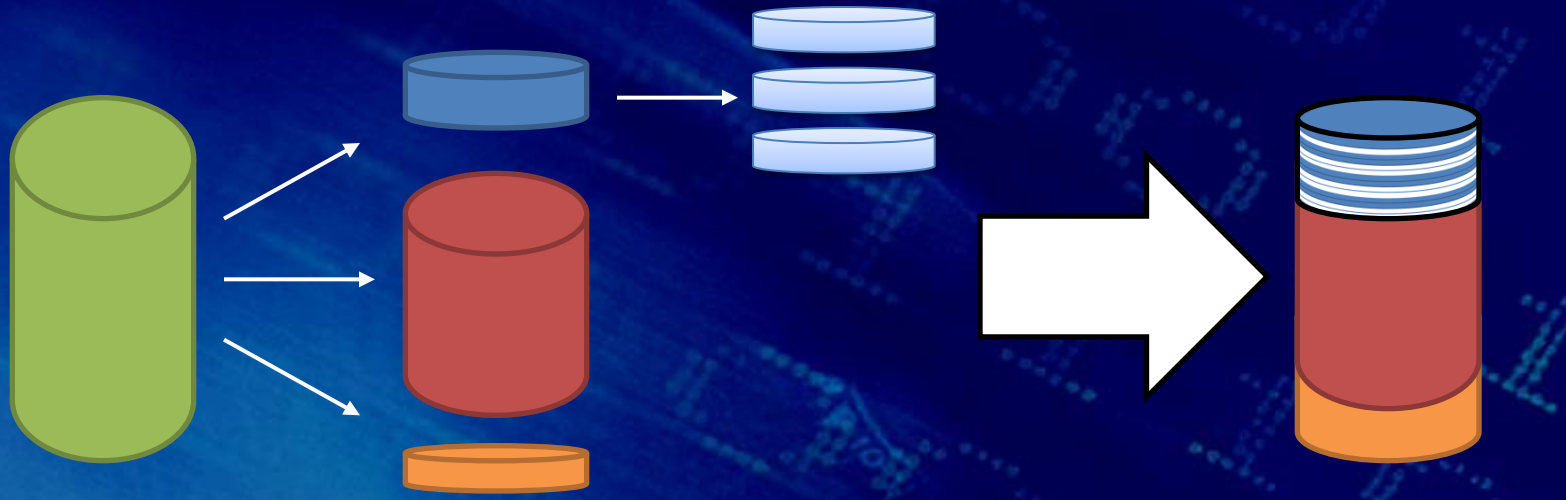
GOAL:

- **Increase the dependability of the partial reconfiguration process by avoiding misreconfigurations**

MY CONTRIBUTIONs:

- **Detecting faults before configuring the FPGA [9] or correcting a misconfiguration [6] with minimal impact**

Mitigating SEE – D²PR [9]



Original Partial Bit File

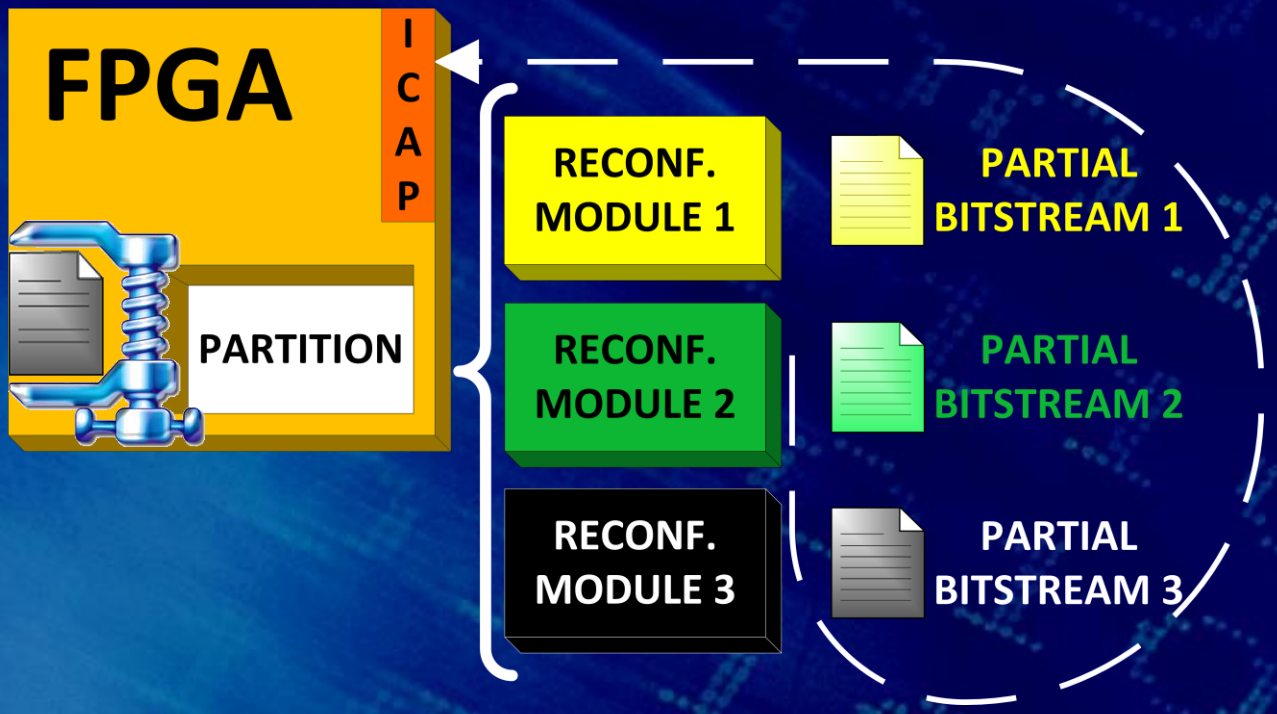
Bit File split into logical Blocks

CRC generated for each word in critical Block

Partial Bit File reassembled with CRC

CRC Signatures are inserted to protect the bitstream addressing and control words, avoiding reconfiguration with faulty data

Mitigating SEE – Zipstream [6]



A special partial bitstream, for each reconfigurable partition, is compressed and stored internally the FPGA, to quickly reconfigure if a faulty bitstream has been read

Aging mitigation by DPR

ISSUE:

- **NBTI induces a degradation of the robustness of the cells by decreasing its Static Noise Margin, especially if the data stored is statically 1 or 0**

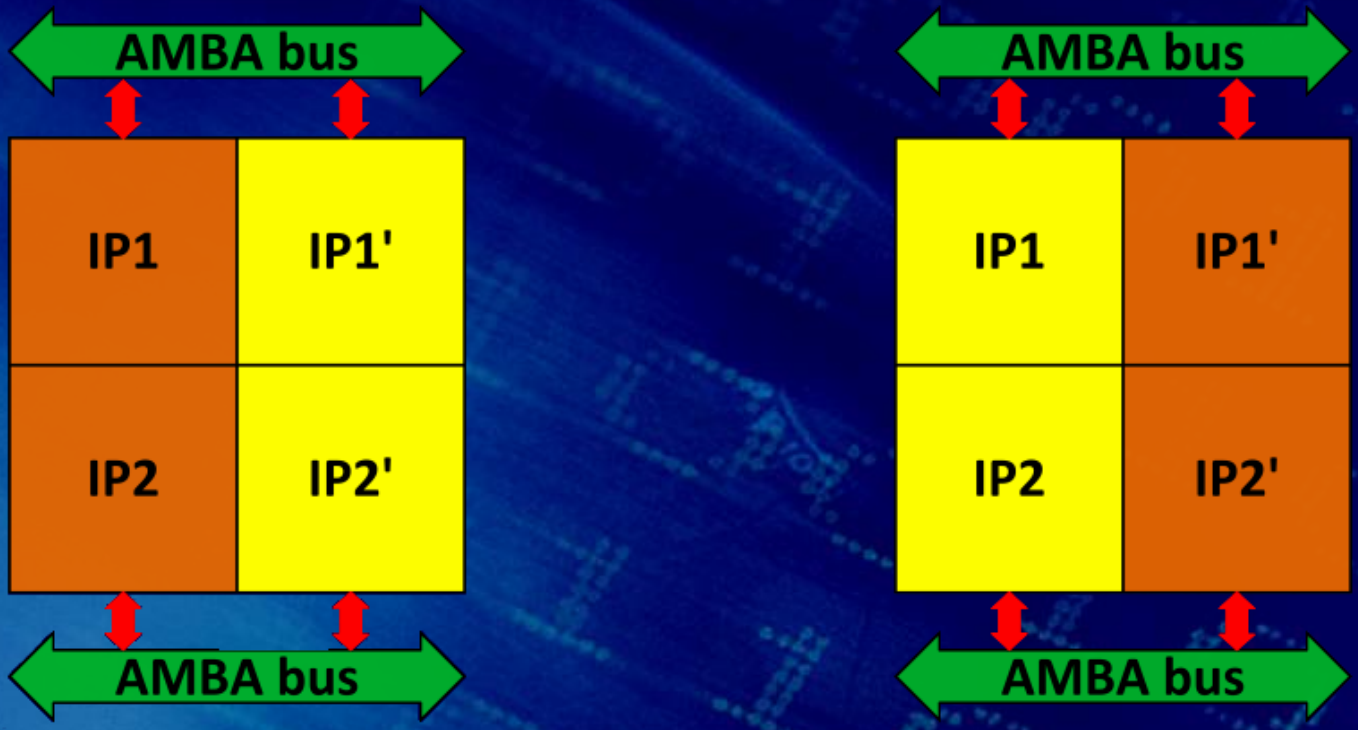
GOAL:

- **Mitigate aging effects in SRAM-based FPGA configuration memory**

MY CONTRIBUTION:

- **By taking advantage of the unused hardware resources and allocating functions to be implemented uniformly into available resources**

Aging mitigation by DPR



By ensuring the 50% probability of having ‘0’ in each configuration memory bits, by switching among two status (Work and Rest), providing the minimum aging effect [5] increasing the SNM

NFPs mitigation by DPR

ISSUE:

- **Non-functional properties (i.e., temperature, power, aging) variations are affecting systems performances and reliability, modifying systems behavior**

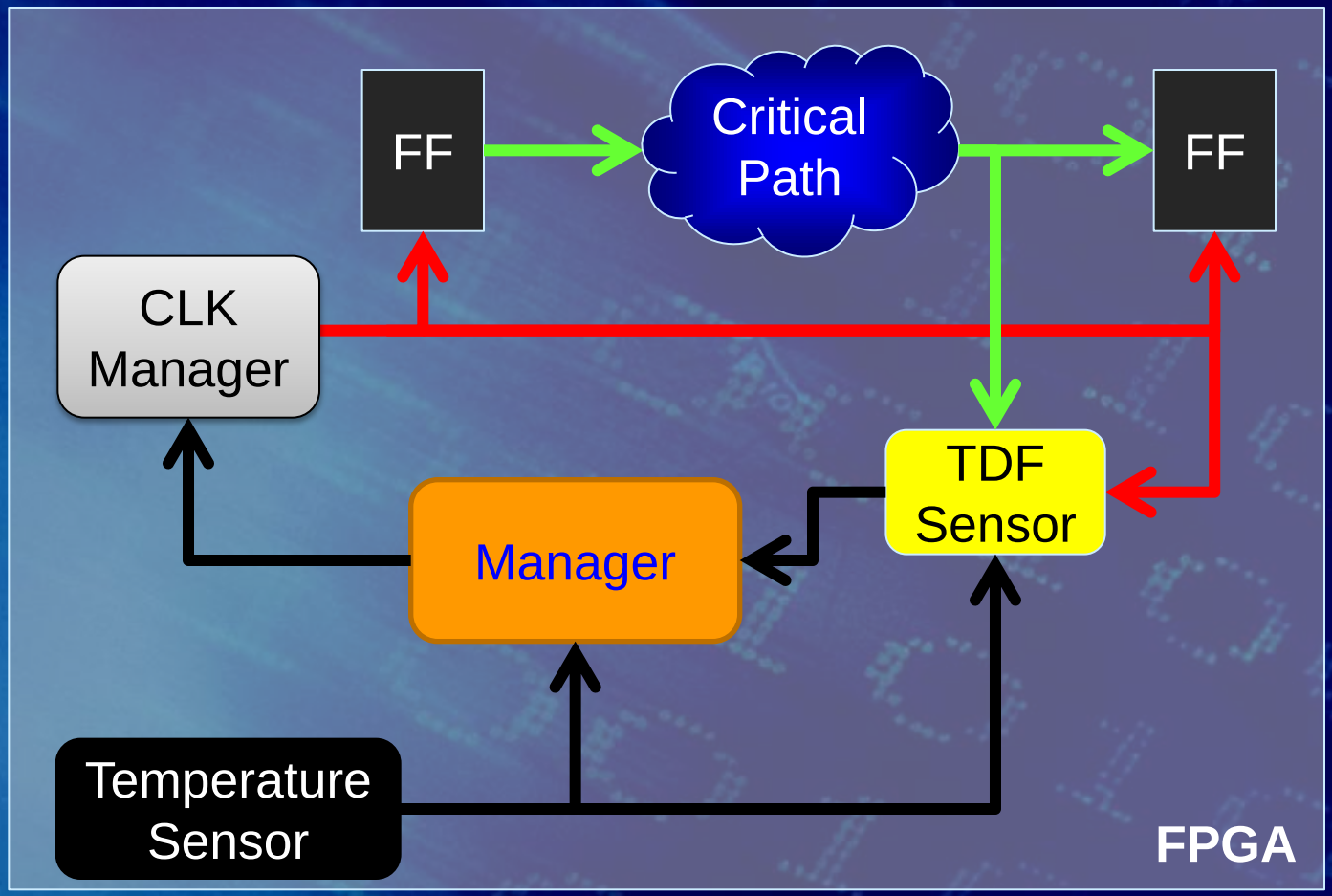
GOAL:

- **Increase Systems-on-Programmable-Chip dependability exploiting DPR**

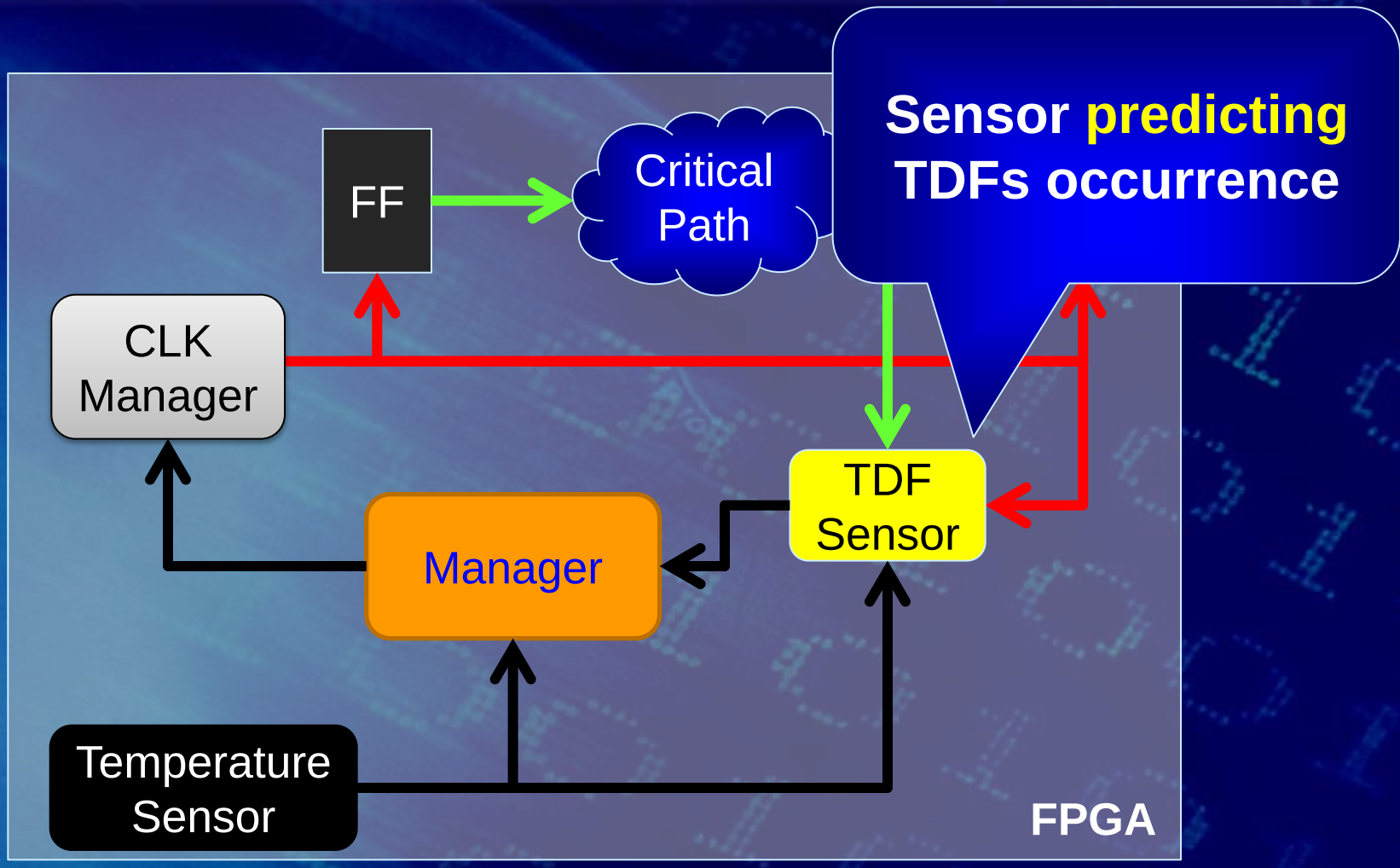
MY CONTRIBUTION:

- **SATTA [13]: a methodology to predict critical path delay changing in FPGA-based system to avoid Transition Delay Faults (TDFs) due to NFPs, integrated into state-of-the-art FPGA design tools**

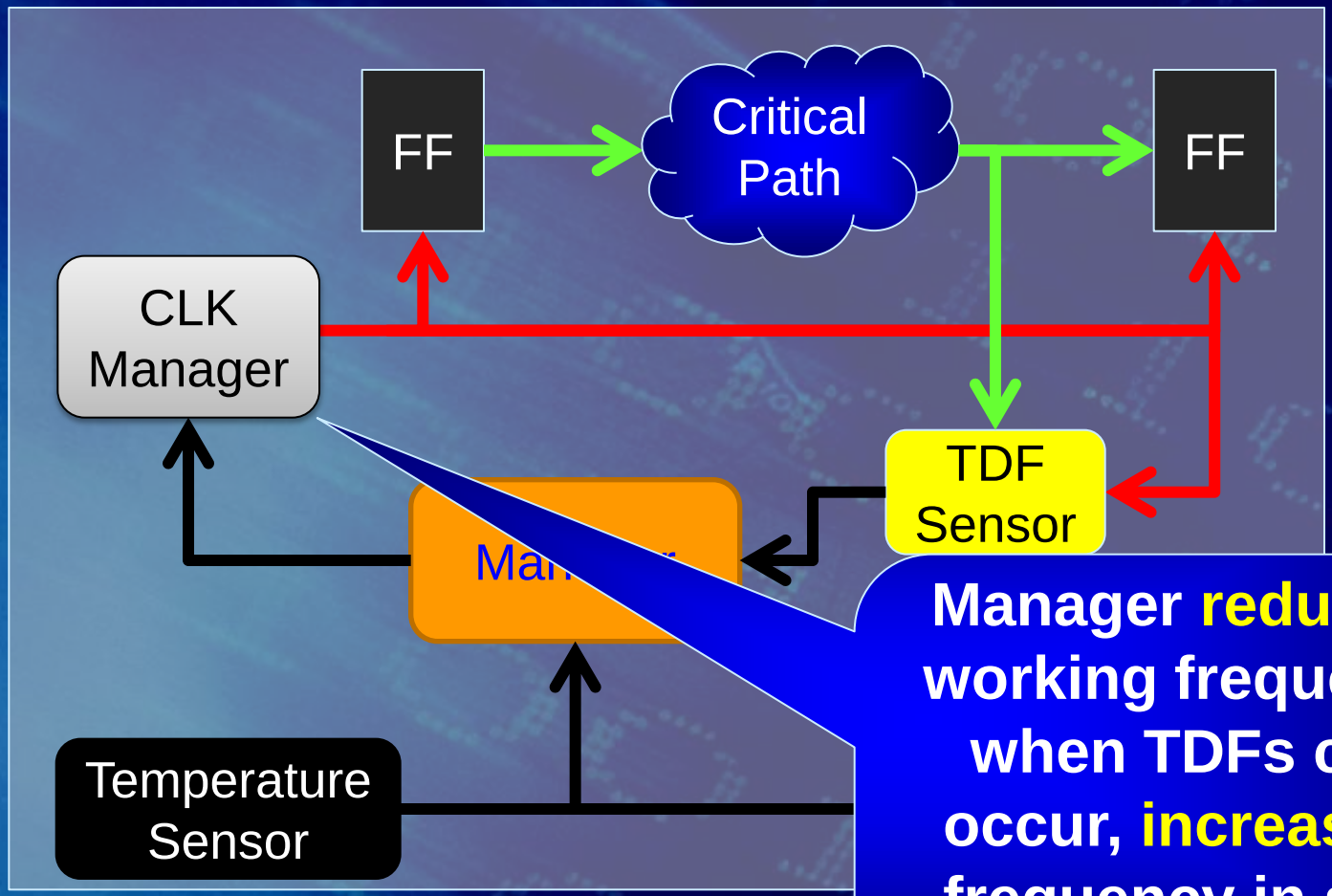
SATTA Architecture



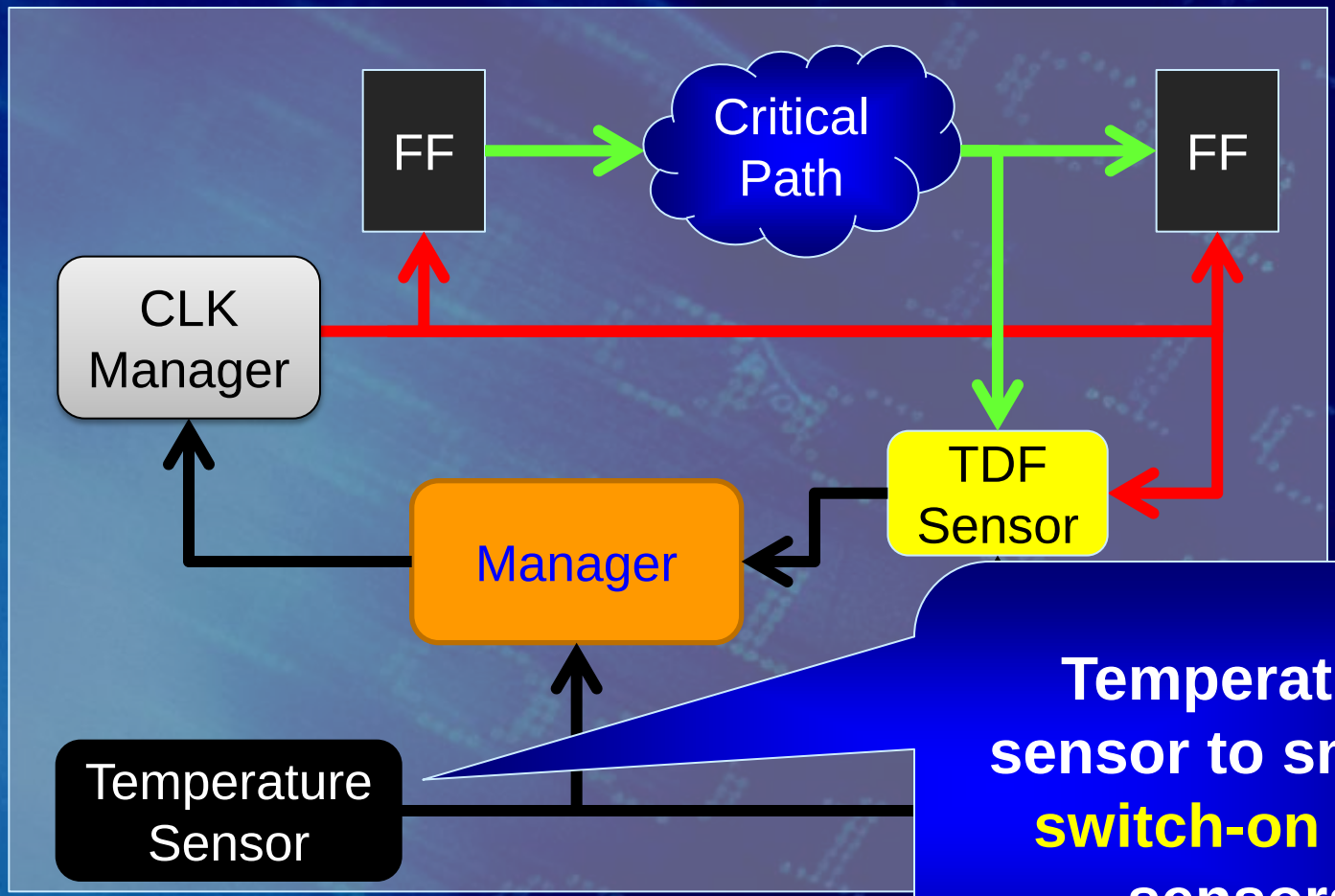
SATTA Architecture



SATTA Architecture

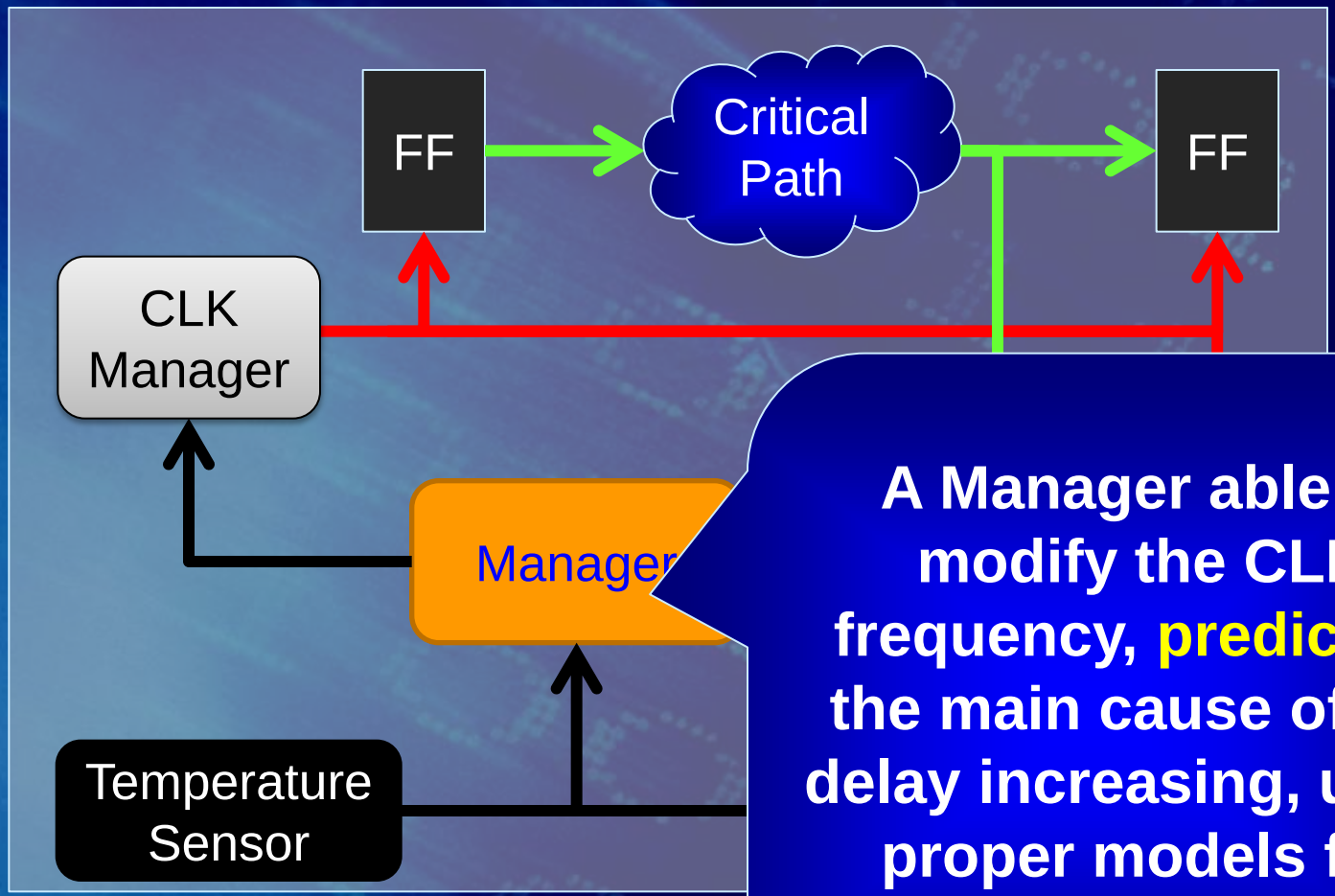


SATTA Architecture



Temperature sensor to smartly switch-on TDF sensors

SATTA Architecture



A Manager able to modify the CLK frequency, predicting the main cause of the delay increasing, using proper models for aging and temperature

Publications – ISI Journals

PUBLISHED:

[13] *"SATTA: a Self-Adaptive Temperature-based TDF awareness methodology for dynamically reconfigurable FPGAs", S. Di Carlo,* ***G. Gambardella****, P. Prinetto, D. Rolfo, P. Trotta; ACM Transaction on Reconfigurable Technology and Systems*

[14] *"SA-FEMIP: A Self-Adaptive Features Extractor and Matcher IP-Core Based on Partially Reconfigurable FPGAs for Space Applications", S. Di Carlo,* ***G. Gambardella****, P. Prinetto, D. Rolfo, P. Trotta; IEEE Transactions On Very Large Scale Integration (VLSI) Systems*

SUBMITTED:

[15] *"MarciaTesta++: A tool for the automated generation of Software-Based Self Tests for both Instruction and Data Cache Memories", S. Di Carlo,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo; Springer Design Automation for Embedded Systems*

Publications – Conferences 2014

[10] *"On Enhancing Fault Injection's Capabilities and Performances for Safety Critical Systems", S. Di Carlo,* ***G. Gambardella****, P. Prinetto, F. Reichenbach, T. Lokstad, G. Rafiq; Proceedings of the Euromicro Conference on Digital System Design (DSD), 2014*

[11] *"A novel methodology to increase fault tolerance in autonomous FPGA-based systems", S. Di Carlo,* ***G. Gambardella****, P. Prinetto, D. Rolfo, P. Trotta, A. Vallero; Proceedings of the International On-Line Testing Symposium (IOLTS), 2014*

[12] *"A cloud-based Cyber-Physical System for environmental monitoring", T. Sanislav, G. Mois, S. Folea, L. Miclea,* ***G. Gambardella****, P. Prinetto; Proceedings of the Mediterranean Conference on Embedded Computing (MECO), 2014*

Publications – Conferences 2013

[8] *"FEMIP: A high performance FPGA-based features extractor & matcher for space applications", S. Di Carlo,* ***G. Gambardella****, P. Lanza, P. Prinetto, D. Rolfo, P. Trotta; Proceedings of the Field Programmable Logic and Applications (FPL), 2013*

[9] *"Dependable Dynamic Partial Reconfiguration with minimal area & time overheads on Xilinx FPGAS", S. Di Carlo,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo, P. Trotta; Proceedings of the Field Programmable Logic and Applications (FPL), 2013*

Publications – Conferences 2012

[5] *"NBTI Mitigation by Dynamic Partial Reconfiguration", S. Di Carlo, S. Galfano,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo, P. Trotta; Proceedings of the 13th Biennal Baltic Electronics Conference (BEC), 2012*

[6] *"ZipStream: improving dependability in Dynamic Partial Reconfiguration", S. Di Carlo,* ***G. Gambardella****, T. Huynh Bao, P. Prinetto, D. Rolfo, P. Trotta; Accepted at 7th IEEE International Design and Test Symposium (IDT), 2012*

[7] *"SAFE: a Self Adaptive Frame Enhancer FPGA-based IP-core for real-time space applications", S. Di Carlo,* ***G. Gambardella****, P. Prinetto, D. Rolfo, P. Trotta; Accepted at 7th IEEE International Design and Test Symposium (IDT), 2012*

Publications – Conferences 2011

[1] *"MarciaTesta: an automatic generator of test programs for microprocessors' data caches", S. Di Carlo,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo; Proceeding of the 20th Asian Test Symposium (ATS), 2011*

[2] *"A unifying formalism to support automated synthesis of SBSTs for embedded caches", S. Di Carlo,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo; Proceedings of the 9th East-West Design & Test Symposium (EWDTS), 2011*

[3] *"Validation & Verification of an EDA automated synthesis tool", S. Di Carlo,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo; Proceedings of the 6th International Design and Test Workshop (IDT), 2011*

[4] *"An Area-Efficient 2-D Convolution Implementation on FPGA for Space Applications", S. Di Carlo,* ***G. Gambardella****, M. Indaco, P. Prinetto, D. Rolfo, G. Tiotto; Proceedings of the 6th International Design and Test Workshop (IDT), 2011*

Q&A

Any Question?